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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/235,615	01/21/99	AGRAWAL	O	AMDI8320MCF/

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EXAMINER	
CHANG, D	
ART UNIT	**PAPER NUMBER**
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/235,615	Applicant(s) Agrawal et al.
	Examiner Daniel Chang	Group Art Unit 2819

☒ Responsive to communication(s) filed on *Jan 21, 1999*.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-21* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-21* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2,3,4*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Specification

1. The specification is objected to because of the inappropriate serial numbers for the cross reference. For example, on page 3, line 8, "Ser. No. 09/xxx,xxx" should be correctly identified.

2. Because of the lengthy specification in this application, it has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is therefore requested in promptly correcting any errors of which he may become aware in the specification or drawings.

Claim Objections

3. Claim 2 is objected to because of a typographical error: "said device" in line 10-11 of the claim 2 appears to be --said field programmable gate array device-- . Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 and 3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. In claim 1, line 26, "the P6 HIC's" lack antecedent basis. It appears to be "the P5 HIC's".

7. In claim 3, line 7-8, "said P3 number" and "the P3 number" lack antecedent basis.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

9. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by McGowan et al. (US PAT. 5,744,980). McGowan et al. shows and teaches all the elements and means of the claimed invention of the claims 1-21:

Regarding claim 1, McGowan et al. discloses a field programmable gate array device (see Fig. 1; col. 3, line 26+) comprising:

a first plurality P1 of repeated logic units (see 12-1, 12-2, ... in Fig. 2; col. 4, line 40+) wherein: each said logic unit is user-configurable to receive and process at least a second plurality P2 of input logic bits (see col. 3, line 41+) and to responsively produce result data having at least a third plurality P3 of output logic bits (see col. 3, line 41+), said logic units are distributed among a plurality of horizontal rows, with each row of the plurality of rows having a fourth plurality P4 of said logic units(see Fig. 2);

a fifth plurality P5 of horizontal interconnect channels (HIC's)(see a, b, c, and d in Fig. 2; col. 4, line 49+) correspondingly distributed adjacent to said horizontal rows of logic units, wherein: each said horizontal interconnect channel (HIC) includes at least P3 interconnect lines(see Fig. 2; col. 3, line 41+), and each said horizontal row of P4 logic units is configurably couplable to a corresponding one of the P[6]5 HIC's at least for receiving input logic bits from the corresponding HIC or at least for outputting result data to the corresponding HIC;

and an embedded memory subsystem(see 16's in Fig. 1; col. 3, line 59+), wherein said embedded memory subsystem includes: a sixth plurality P6 of memory blocks(see 16-1, 16-2, ... in Fig. 2) and wherein: each said memory block is embedded within one of said rows of logic units and is configurably couplable to the corresponding HIC of said row for transferring storage data by way of the corresponding HIC of that row of P4 logic units(see Fig. 2; col. 5, line 1+); each of said memory blocks includes at least a first address-capturing register (34 in fig. 3) that is programmably couplable to at least one of said HIC's for receiving and capturing an address signal (36) supplied on said at least one HIC.

Regarding claim 2, McGowan et al. discloses a FPGA device according to Claim 1 wherein:

said logic units are further distributed among a plurality of vertical columns, with each column of the plurality of columns having a fifth plurality P5 of said logic units(see

Fig. 2); and plural ones of said memory blocks are arranged to define one or more columns of embedded memory within said device with each such column having an eighth plurality P8 of said memory blocks (see Fig. 1; col. 3, line 59+).

Regarding claim 3, McGowan et al. discloses a field programmable gate array device according to Claim 1 wherein:

each said memory block is organized as a ninth plurality P9 of addressable sets of storage data bits(see Fig. 3; col. 6, line 56+), where each addressable set of storage data bits includes at least P3 bits, said P3 number corresponding to the P3 number of output logic bits producible by each said logic unit.

Regarding claim 4, McGowan et al. discloses a field programmable gate array device according to Claim 2 wherein: each of P2 and P3 is an integer equal to or greater than 4 (see col. 4, line 53+).

Regarding claim 5, McGowan et al. discloses a field programmable gate array device according to Claim 1 wherein:

groups of said logic units are further wedged together such that each group of logic units defines a logic superstructure; and groups of said memory blocks are also wedged together such that each group of memory blocks defines a memory superstructure that is configurably couplable to a corresponding logic superstructure (see Fig. 2; col. 4, line 40+, col. 7, line 19+).

Regarding claim 6, McGowan et al. discloses a field programmable gate array device according to Claim 1 wherein said embedded memory subsystem includes: at least one special interconnect channel(see 18-n in Fig. 3; col. 7, line 40+) for supplying address signals to the first address-capturing registers of a respective set of said memory blocks.

Regarding claim 7, McGowan et al. discloses a field programmable gate array device according to Claim 6 wherein: there are at least two of said columns of embedded memory(see Fig. 1; col. 3, line 61+); and there are at least two of said special interconnect channels, and each respective special interconnect channel is for supplying address signals to a respective one of the at least two columns of embedded memory(see 18-n in Fig. 3; col. 7, line 40+).

Regarding claim 8, McGowan et al. discloses a field programmable gate array device according to Claim 6 wherein:

each said memory block has at least first and second data ports each for outputting storage data(see 5 and 6 in Fig. 2; col. 5, line 50+);

each said memory block has at least first and second address ports each for receiving address signals identifying the storage data to be output by a corresponding one of the at least first and second data ports (see 1, 2, 3, and 4 in Fig. 2; col. 5, line 31+);

each said memory block has in addition to said respective first address-capturing register, a second address-capturing register (54 in fig. 3) that is programmably couplable to at least one of said HIC's for receiving and capturing an address signal supplied on said at least one HIC, and said first and second address-capturing registers respectively service the first and second address ports; and

the at least one special interconnect channel includes first and second address carrying components along which independent address signals may be respectively carried for application to respective ones of the first and second address ports of at least two memory blocks (see 18-n in Fig. 3; col. 7, line 40+).

Regarding claim 9, McGowan et al. discloses a field programmable gate array device according to Claim 1 wherein:

each said memory block has a controls receiving port for programmably acquiring control signals that control operations of said memory block (see 1, 2, 3, and 4 in Fig. 2; col. 5, line 31+); and each respective first address-capturing register is clocked by a respective first address clock signal (46, 46, 38) acquired by said controls-receiving port.

Regarding claim 10, McGowan et al. discloses in a field programmable gate array device (FPGA)(see Fig. 1) having a user-configurable interconnect network that includes a plurality of horizontal interconnect channels(see Fig. 2; col. 3, line 41+) each with a

diversified set of long-haul interconnect lines and shorter-haul interconnect lines, an embedded memory subsystem comprising:

a plurality of multi-ported memory blocks each arranged adjacent to a horizontal interconnect channel (HIC) of the interconnect network(see Fig. 2; col. 5, line 1+); wherein: each multi-ported memory block includes a first, independently-addressable data port and a second, independently-addressable data port(see 1, 2, 3, and 4 in Fig. 2; col. 5, line 31+); each of said first and second, independently-addressable data ports includes a respective address-capturing register (34, 54) that is connectable by user-configurable intercouplings to one or both the long-haul interconnect lines and the shorter-haul interconnect lines(see 1, 2, 3, and 4 in Fig. 2; col. 5, line 31+) for capturing a respective address signal.

Claims 11-13 are essentially the same in scope as apparatus claim 10 and are rejected similarly.

Method claims 14-21 are essentially the same in scope as apparatus claims 1-13 and are rejected similarly.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cliff et al. (US PAT. 5,689,195 and 5,828,229) discloses a programmable logic array integrated circuit having RAM and address registers.

Bauer (US PAT. 5,787,007) discloses a structure and method for loading RAM data within a programmable logic device.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ***Daniel D. Chang*** whose telephone number is (703)306-4549. The examiner can normally be reached between the hours of 6:30 AM to 4:00 PM Monday thru Thursday and every other Friday (first Friday of the bi-week).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Daniel D. Chang
Patent Examiner, Art Unit 2819
June 21, 2000

Michael J. Tokar

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